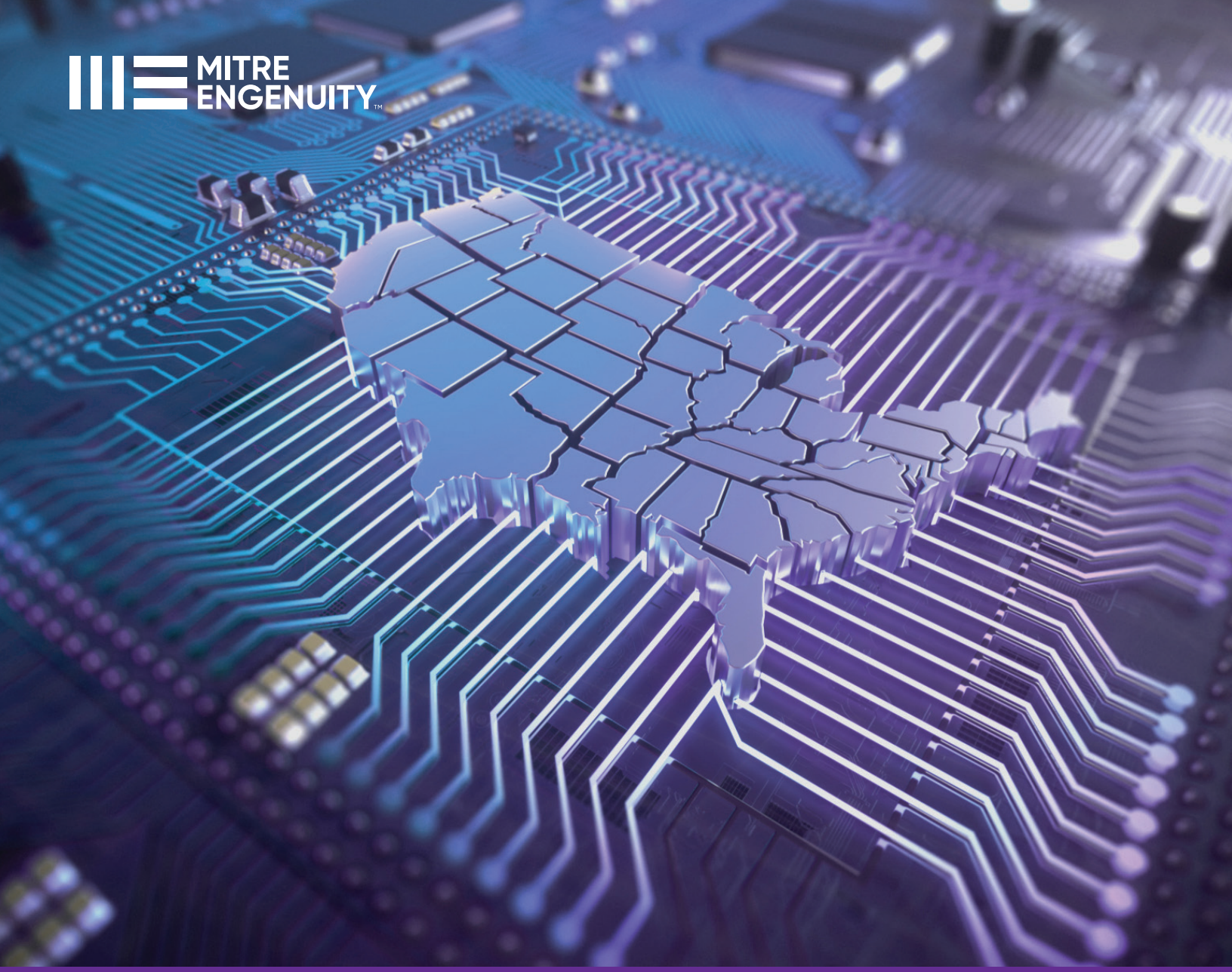

MITRE ENGENUITY™

AMERICAN INNOVATION, AMERICAN GROWTH:

A VISION FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER

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EXECUTIVE SUMMARY

The 2021 National Defense Authorization Act's call to create a National Semiconductor Technology Center (NSTC) is a unique opportunity to strengthen the United States' ability to translate American semiconductor innovation into manufacturable, market-ready technology domestically. The success of the U.S. economy is connected to our ability to translate world-class science and technology into new business, jobs, prosperity, and opportunities for further innovation. Today, promising basic research in microelectronics often dies on the vine, is taken up by foreign entities, or falls into the "valley of death" due to inadequate domestic funding and access to resources and fabrication facilities (fabs) that are needed to scale innovations to commercialization.

Moreover, the U.S. lacks mechanisms for coordinating "full-stack" approaches to next-generation technology development. The next paradigm shift in computing technology will require complementary innovations across the compute stack (i.e., in materials, devices, process technologies, architectures, software, applications, etc.). However, as a result of decades of industry consolidation and specialization, no single company has the skills and resources necessary to innovate across the full stack. The U.S. needs a National Semiconductor Technology Center capable of aligning diverse organizations around common objectives and coordinating cross-sector full-stack approaches to innovation.

To address these challenges, The MITRE Corporation's neutral, not-for-profit technical foundation for public good, MITRE Engenuity, has launched The Semiconductor Alliance - a group that consists of leading organizations in the U.S. semiconductor industry. Together, MITRE Engenuity and The Semiconductor Alliance have developed a vision and framework for the NSTC to ensure that it addresses the dual challenges of bridging the valley of death and driving full-stack innovation. Our core objective is to ensure that American innovation leads to American growth. To achieve that objective, the NSTC must ensure the following:

- **A Marketplace of Competitive Ideas**
  Launch Breakthrough Challenges that align industry around revolutionary – not evolutionary – goals, coordinate development across the compute stack, and foster competition of ideas
- **A Whole-of-Nation Effort**
  Develop a nationwide network of existing facilities to support the NSTC's work in the most cost-effective and timely manner, while also seeking to construct or acquire new facilities if critical gaps remain that affect the NSTC's ability to achieve its technical missions
- **High-Impact Investment and Incubation**
  Establish an investment fund that both fills emerging companies' need for capital and acts as an incubator, connecting companies with resources and facility access to de-risk their technology maturation
- **A Workforce of the Future**
  Invest in a robust domestic semiconductor workforce through curriculum development, internship and job opportunities, scholarships, vocational training programs, and K-12 educational resources
- **Neutral, Balanced, and Resilient Governance**
  Ensure that the NSTC has an effective governance model that mitigates conflicts of interest and ensures that the NSTC remains focused on the good of the nation and the U.S. semiconductor industry overall, rather than on the interests of any particular entities or regions
- **Accountability to U.S. Government Objectives**
  Coordinate with existing and future U.S. government programs - including those described in the 2021 National Defense Authorization Act (NDAA) - to ensure that investments are mutually reinforcing and make most effective use of taxpayer funds

The organizations selected to establish the NSTC must be held accountable for delivering demonstrable benefits to U.S. economic development and national security. **MITRE Engenuity** and **The Semiconductor Alliance** are ready and able to take up this mantle of responsibility in service to our nation.

Introduction and Context

American innovation should lead to American growth. For the complex global semiconductor industry, effectively translating innovation into domestic growth requires strategic and targeted investments. There is no question that the United States is the global powerhouse for semiconductor research and development (R&D). Over the past decade, the U.S. has invested nearly twice as much in R&D as the rest of the world combined.[1] By many measures, American innovation *is* leading to American growth. In 2015, the U.S. was home to half of the world's top 20 semiconductor companies by revenue and accounted for roughly 50% of global sales.[2] However, beneath those numbers lies a more complicated, shifting competitive landscape.

From the time it is specified in a design to the time it is sold to a customer, a single semiconductor chip can progress through over 1,000 production steps and cross 70 international borders.[3, 4] Some of those steps happen on allied or U.S. soil, but many – notably manufacturing – have been offshored. The U.S. currently only holds 12% of global semiconductor manufacturing capacity – down from 37% in 1990 – and does not have the most advanced fabrication nodes.[5] By contrast, Taiwan, home to Taiwan Semiconductor Manufacturing Company (TSMC), accounts for 47% of manufacturing capacity for advanced (≤10nm) logic semiconductors.[6] China is leveraging $150 billion to gain 40% of the world's new manufacturing capacity by 2030, bringing its expected market share up to 25%.[7, 8]

However, while the U.S.'s growing manufacturing dependency may be the most apparent and popularly discussed threat to its ability to turn American innovation into American growth, it is just one piece of the puzzle. The U.S. can lose the value of its innovation not only by ultimately relying on foreign entities to manufacture the technologies, but also by underinvesting in developing breakthrough ideas and maturing them to the point of manufacturability domestically. To ensure that American innovation can grow from "lab to fab" domestically, the U.S. needs to make substantial, sustained, and smart investments in building domestic capacity for prototyping and scaling breakthrough semiconductor technologies. The need for these investments is more urgent than ever, as existing semiconductor technology is rapidly approaching the physical limits of two-dimensional scaling underpinning Moore's Law. The end of two-dimensional scaling will necessitate a fundamental reinvention of semiconductor logic, and the rapid growth in artificial intelligence (AI), the internet of things, and communications technologies will require groundbreaking innovation in analog and memory technologies as well.[9] Only by out-innovating its competition and capturing the value of that innovation domestically will the U.S. be able to secure its semiconductor leadership in the decades to come.

The 2021 National Defense Authorization Act (NDAA) has created an opportunity for the U.S. to begin making these critical investments.[10] In addition to calling for funding incentives to onshore manufacturing and to collaborate with allies, the NDAA calls for the creation

of a National Semiconductor Technology Center (NSTC) that will "conduct research and prototyping of advanced semiconductor technology to strengthen the economic competitiveness and security of the domestic supply chain."[11] Projected appropriations for the NSTC and related efforts amount to $10.5 billion.[12] However, despite these billions of dollars of anticipated appropriations, the NDAA provides little detail about what the specific focus of the NSTC should be, how it should work, how and with whom it should partner, how it should measure its success, and how it should relate to and complement other existing and planned U.S. government investments.

In this paper, MITRE Engenuity and The Semiconductor Alliance take on the task of defining the principles by which the NSTC should be established to ensure that the U.S. makes the most of this opportunity to bring substantial funding and cross-sector collaboration to bear on the challenge of driving U.S. leadership in semiconductors for decades to come.

Our Approach and Unique Perspective

Because the semiconductor industry is so large, diverse, and critical to both U.S. economic and national security interests, investments in the NSTC need to be shaped by a strategic, cross-sector set of stakeholders. The NSTC is not something that the U.S. can afford to allow to be defined by and tailored toward narrow interests.

The perspectives that MITRE Engenuity and The Semiconductor Alliance share in this paper are particularly valuable because they exemplify:

- **Strategic, Cross-Sector Participation**
  MITRE Engenuity convened a diverse group of experts from over 10 major U.S. semiconductor companies that span the semiconductor value chain – from design to equipment to semiconductor manufacturing – and that represent the logic, memory, and analog market segments to form the core working group of The Semiconductor Alliance. We also engaged regularly with startups, universities, major industry associations, investors, and stakeholders from across government to ensure that our work considered the perspectives of all facets of the U.S. semiconductor ecosystem.
- **Neutral Facilitation and Management**
  MITRE Engenuity – which convened The Semiconductor Alliance, facilitated its work, and consolidated its findings in this paper – is an impartial, independent, and objective not-for-profit organization with experience working in advanced technologies for the public interest and has no financial stake in the semiconductor industry. As such, MITRE Engenuity was able to act as an objective mediator of different perspectives and built consensus around common themes and ideas.
- **Attention to Best Practices and Lessons Learned from Other Organizations**
  Because we undertook this effort in an open-minded, neutral way with a broad set of collaborators, we were able to adopt best practices and lessons learned from a variety of past and existing organizations and programs to inform our recommendations. Our case studies of other organizations covered governance, business models, technical missions, and infrastructure assets. Key learnings from these case studies appear throughout the paper to illustrate and to strengthen our recommendations.

The results of our work are:

- A clear statement of the problem and most critical ecosystem gaps that the NSTC must address, which reflects both the perspectives of the U.S. semiconductor industry and the language of the 2021 NDAA
- The value proposition and differentiation of the NSTC within the U.S. semiconductor ecosystem
- Key principles for implementing the NSTC, along with a discussion of how the NSTC should function and how it should coordinate with other U.S. government initiatives and programs in advanced semiconductor technologies
- Milestones to which the NSTC should be held accountable to ensure that the U.S. government's substantial investment demonstrably improves U.S. economic resiliency and national security

Addressing a Vital Problem for U.S. Competitiveness

The Problem Statement

U.S. leadership in semiconductors is threatened by **the lack of U.S.-based capacity for prototyping,[13] scaling,[14] and transfer-to-manufacturing of breakthrough semiconductor technologies** that are the foundation of future information and communications solutions necessary for national security and economic resiliency.

To secure U.S. leadership in the next generation of semiconductor technologies, it is critical to strengthen the U.S.'s ability to translate its world-leading R&D into mature, manufacturable technological innovations domestically. The U.S. is already in a strong position to lead the design of the next generation of semiconductor technologies. The U.S. has led the rest of the world combined in semiconductor R&D funding over the past decade, is home to many of the world's leading R&D universities, and leads the market for electronic design automation tools (96% market share), manufacturing equipment (52%), and core IP (52%).[15, 16] However, two distinct difficulties limit the rate at which novel ideas turn into commercial competitive advantage for U.S. industry:

The Difficulty of Bridging the "Valley of Death"

For every breakthrough technology that the U.S. semiconductor industry successfully brings to market, there are plenty of other promising innovations that never make it out of research laboratories. Instead, they fall into the "valley of death" – a term which refers to "the lack of funding or investment for the middle stages of developing a technology or product" that often results in early-stage technologies being shelved indefinitely or prematurely abandoned.[17] University research and government-funded programs - e.g., through the National Science Foundation (NSF) and the Department of Energy (DOE) - tend to focus on fundamental research, early idea development, and laboratory proof of concept demonstrations. The Semiconductor Research Corporation (SRC) also sponsors this type of university research. Other government

funding - e.g., through the Defense Advanced Research Projects Agency (DARPA) - is project-driven and mission-focused, and the degree to which it addresses technology maturation and scaling is variable. These funding sources generally stop short of demonstrating the scalability and process integration necessary to bridge from demonstration in a laboratory to production in a manufacturing facility. Industry, on the other hand, largely tends to focus on technologies that already have demonstrated some ability to scale beyond laboratory environments and, thus, are relatively low-risk investments. Currently, there is only a handful of companies in the U.S. (e.g., Intel and Micron) with the resources, infrastructure, and expertise to bridge the gap between where basic research funding ends and where industry invests in transitioning technology to commercial production. Venture capital (VC) sometimes fills the funding gap in other industries, but VC funding in the semiconductor industry has drastically declined.[18] Investors tend to prefer software-driven companies with fast time-to-market, five- to seven-year exit horizons, low capital expenditures, and low technical risk. In the semiconductor industry, breakthrough technologies typically take over 10 years to become commercially marketable, manufacturing fabs cost billions of dollars, and technical risk is high. Without investment, many ideas have no domestic path from "lab to fab to market."

It is important to note that funding – while critical – is not the only thing that companies need to shepherd new technologies through the valley of death to commercial launch. It is equally critical to have access to facilities, tools, and personnel suitable for demonstrating the ability to produce an innovation at commercial scale. Even well-funded startups often struggle to secure wafer runs at contract user facilities or foundries – in some cases, because they compete and lose against larger companies for access, as noted in **Exhibit 1**. If innovations require changes to the process of record, access is exceptionally difficult to secure. While some prominent market leaders have their own corporate facilities for prototyping and scaling novel technologies, they tend to be the exception rather than the rule, and these facilities are typically not accessible to external teams. Consequently, many large companies also often struggle to find suitable facilities in which to prototype and scale innovations.

The danger of underinvesting in bridging the valley of death is not just that promising innovations are left on the shelf, but also that other countries, notably China, are able to seize the opportunity to commercialize and to capitalize on U.S. innovation. China invests

Insufficient Funding	Competing for Facility Access	Delayed Time-to-Market
In addition to the scarcity of venture capital investment in semiconductor startups, existing government funding programs are falling short of meeting startups' needs. One corporate spinout developing disruptive new technologies reported that a total of five Small Business Innovation Research (SBIR) grants still amounted to less than the cost of running one lot of wafers at Imec.	One series B company with roughly $90M in funding reported losing a deposition slot it had reserved at an R&D foundry to a larger Chinese company. Startups report that this is a common occurrence.	Startups reported that inability to access cleanroom space at fabs leads to substantial delays in preparing their innovations for market. One company that has raised over $100M estimated that lack of facility access has delayed its time-to-market by two years.

EXHIBIT 1. STARTUP PERSPECTIVES & CHALLENGES

aggressively in acquiring foreign companies, intellectual property (IP), and equipment to build its own domestic semiconductor industry. The China Integrated Circuit Investment Industry Fund (CICIIF) marshals $150 billion in funding for these purposes. China has continued to expand this investment, creating another $28.9 billion semiconductor fund in 2019.[19] If promising IP and high-potential startups cannot find the support they need to grow in the U.S., they may increasingly find the funding they need from China.

The Complexity of Exploration and Pursuing "Full-Stack" Innovation

To achieve truly next-generation technological advancements, companies must undertake bold exploration and take risks.[20] It is not enough to iteratively develop aspects of new technologies in isolation. Rather, it is critical to explore revolutionary new ideas that will require many elements to come together to create a functional new technology. These elements comprise the "compute stack" (see **Exhibit 2**). To understand what "full-stack" innovation – that is, innovation across all the elements of the compute stack – entails, consider the creation of smartphones. In order to reinvent the cell phone to function like a handheld computer, mobile handset equipment manufacturers had to incorporate innovations at every layer of the compute stack.

Similarly, full-stack innovation is critical to developing the next generation of semiconductors and semiconductor-enabled technologies, including – but not limited to – the next generation of processing units for AI, in-memory compute, quantum computers, and packaging. Packaging has grown in

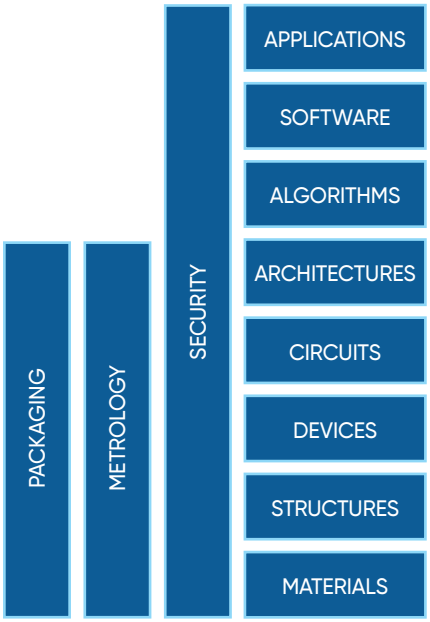

EXHIBIT 2. THE COMPUTE STACK[21]

importance as one of the key technology enablers to compensate for the slowing of two-dimensional scaling. Moreover, taking a full-stack approach is important to ensure that next-generation technologies are secure. Attackers often find the weakest link in the stack to gain access to and to undermine a system. When a new system is created in a piecemeal fashion, rather than with attention to the full stack, there tend to be more security gaps between the different elements it comprises. Full-stack innovation is key to ensuring that the U.S. can develop sophisticated, next-generation technologies that are secure for both private and government users.

The difficulties that the U.S. semiconductor ecosystem faces are two-fold. First, leading U.S. companies tend to exploit existing know-how, rather than exploring bold but risky initiatives that will upend the compute stack and usher in

next-generation computing paradigms. Second, companies also tend to specialize in a subset of the stack, and there is no coordinating entity in the semiconductor industry to drive and to enable collaborative, full-stack innovation. This is especially true when new semiconductor materials and processes are needed to enable new solutions. Without well-defined, coordinated, and resourced collaboration across organizations to develop breakthrough technologies, it is more difficult to pursue revolutionary ideas and less efficient to integrate innovations in individual elements into functional end-user solutions down the line.

In summary, as illustrated in **Exhibit 3**, the lack of an entity that can coordinate innovation across the full-stack and carry that innovation from laboratory demonstrations to readiness for high-volume manufacturing limits the U.S.'s ability to turn American innovation into American growth.

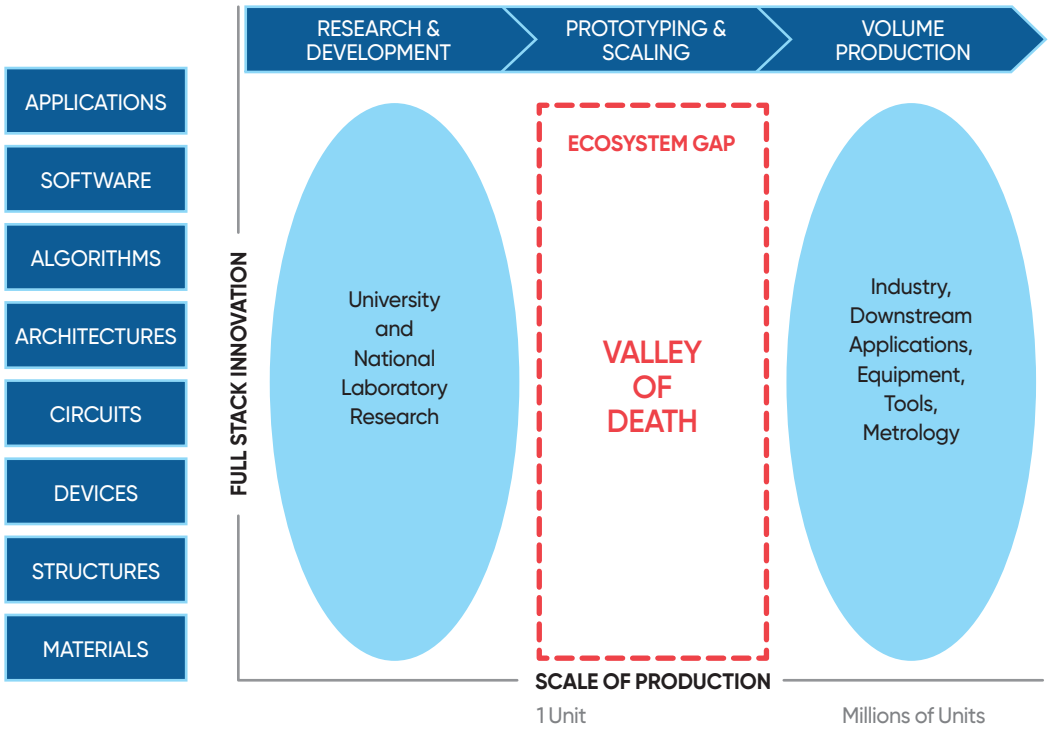

EXHIBIT 3: MAPPING THE ECOSYSTEM GAP

The NSTC's Value Proposition

The NSTC should augment U.S. national security and economic resiliency by **enabling industry to solve multidisciplinary problems and to prototype and scale critical, emerging semiconductor technologies to domestic production** in the U.S.

The creation of an NSTC provides a unique opportunity to fill the ecosystem gap, as shown in **Exhibit 4**.

The NSTC's differentiation should be its ability to mitigate development risk for revolutionary new technologies by providing the infrastructure, multidisciplinary partnerships, industry-driven agenda, and risk mitigation necessary to transition technologies to commercial industry. The following sections elaborate on this vision for the NSTC, providing overall keys to success and roadmaps for each of the NSTC's core functions.

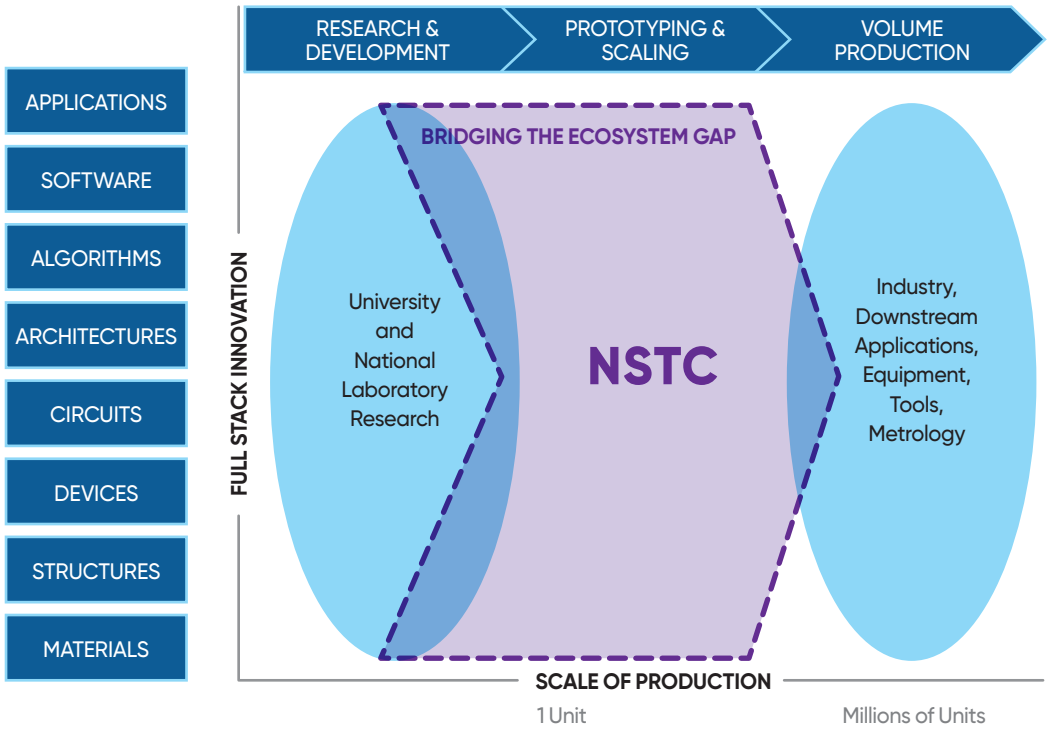

EXHIBIT 4: THE NSTC FILLS THE ECOSYSTEM GAP

Creating the NSTC

To create an NSTC capable of filling the aforementioned ecosystem gap and answering the NDAA's explicit call to do work that "strengthens the entire domestic ecosystem," we need to think outside the box and not be limited by the scope and interests of existing organizations or initiatives.[22] Our recommendations are shaped by the following principles:

- The NSTC needs **effective governance** to ensure that it does not become mired in narrow interests, conflicts of interest, or short time horizons.
- In order to fill ecosystem gaps, the NSTC should be focused on **revolutionary, not evolutionary, innovation** in **various types of semiconductors** (e.g., not only leading-edge logic) and should drive **collaborative, full-stack innovation.**
- There should be mechanisms for **both startups and established companies** to participate in the NSTC to capture breakthrough innovations from many sources.
- The NSTC should **launch breakthrough challenges that promote competition of ideas** to ensure that the NSTC invests in vectors that are most technically promising and commercially impactful and does not put all of its eggs in one basket.
- The NSTC should transition breakthrough technology from **"lab to fab,"** thereby enabling domestic manufacturing of U.S. innovations.
- To use its resources most effectively, the NSTC should **leverage relevant existing facilities from across the nation, constructing or acquiring new infrastructure** to fill gaps, as needed, to achieve its technical missions.
- All of the functions of the NSTC – technology prototyping and scaling, investment, and workforce development – should **fit together in mutually reinforcing ways and should also be mutually reinforcing with existing and future government and industry investments.**

From these core principles, MITRE Engenuity and The Semiconductor Alliance have developed a set of recommendations to shape the governance and core functions of the NSTC. The approach we outline here will ensure that the NSTC substantially improves the ability to translate American innovation into American growth.

Establishing Effective Governance

Effective governance is not a mere implementation detail; it is critical to the success and sustainability of the NSTC. It is the foundation upon which the NSTC will succeed or fail. MITRE Engenuity and The Semiconductor Alliance offer several recommendations for shaping the NSTC's governance, which are based on careful study of best practices and challenges from past and existing technology development-focused organizations listed in **Exhibit 5**.

SEMATECH (U.S.)	Fraunhofer-Gesellschaft (Germany)
Imec (Belgium)	AIM Photonics (U.S.)
Semiconductor Research Corporation (U.S.)	NextFlex (U.S.)
VLSI (Japan)	DOE National Labs (U.S.)

EXHIBIT 5: GOVERNANCE CASE STUDIES

The NSTC should be operated as an independent, objective, and neutral not-for-profit to guarantee that it acts in the interests of the general public and, in turn, U.S. economic leadership. As an independent not-for-profit, the NSTC should have its own bylaws, governance, and board of directors. To ensure that the NSTC executes its strategy effectively and avoids becoming consumed by market-specific or short-term interests or conflicts of interest, the NSTC's governance should reflect five primary concepts: (i) neutral leadership; (ii) no single entity with a controlling position on the board; (iii) periodically refreshed leadership perspectives; (iv) authority for leadership to make strategic decisions quickly; and (v) continuing review of NSTC operations to adapt to changing market and environmental conditions. The following paragraphs elaborate on these concepts:

Require that the chairperson of the board of directors always be a neutral party with no connection to a specific industry or stakeholder perspective

A common theme among organizations with effective boards is the presence of neutral representatives who can moderate and reconcile different interests and who can ensure that all board members work toward the best outcomes for the organization overall, rather than for individual stakeholders.

Among the organizations we studied, those with an independent board chair or other independent board members were better served by their boards of directors. This is due to the moderating influence of the neutral party on the other board members to vote in the interest of the organization, ensuring the organization has the resources and leadership to achieve its mission. In contrast, organizations for which all the board members represented dues-paying member companies suffered from board members' prioritizing the interests of their parent companies.

Ensure that no single entity has a controlling position on the board and that policies exist to mitigate conflicts of interest

No single entity or group of entities should have a controlling stake on the board to co-opt decisions of the NSTC. Semiconductors are critical to U.S. national security, and the government is projected to provide substantial funding for the NSTC. As such, there should be mechanisms for technical experts from the government to provide input on the NSTC's technical priorities. These mechanisms for input should be similarly robust for industry participants who will provide resources, capabilities, and funding to the NSTC. However, there are compelling reasons to avoid giving either government or industry a controlling position on the NSTC's board.

Government representation on the board could create conflicts of interest if the NSTC decides to compete for additional government funding in the future. In such a situation, persons from the same departments and agencies potentially would be sitting on both sides of the table – as bidder and evaluator.

Additionally, large industry stakeholders who will contribute resources and funding to establish the NSTC in partnership with the government should not have a controlling stake on the board of directors. The NSTC must serve the interests of many stakeholders from across the semiconductor ecosystem. This is best accomplished by a balanced board of directors driving consensus across diverse perspectives.

Implement term limits on board members and consider rotation of board members across various industry stakeholders to reflect diverse viewpoints from across the entire semiconductor value chain

To ensure fresh perspectives on the NSTC's board, there should be term limits on board members' service. While finite term duration is important, term limits should be several years long to enable board members to contribute substantively to the NSTC. Rotating board membership to include representatives from across the semiconductor value chain will ensure that the NSTC reflects diverse perspectives.

Authority and agility for leadership to make and execute strategic decisions quickly within the NSTC's non-profit mission and risk tolerance

The NSTC's Chief Executive Officer (CEO) and leadership team must have the ability to make decisions quickly and to implement those decisions rapidly. The NSTC must operate efficiently to maintain relevance with the market-competitive semiconductor industry and, as such, should not be slowed by undue bureaucracy. Thus, within the scope of its mission and a well-defined level of risk tolerance, the NSTC's leadership must be empowered with the authority and independence to take action.

Re-evaluate governance periodically to ensure that the NSTC is able to adapt to evolving missions and the semiconductor ecosystem over time

If government and industry intend for the NSTC to become a long-term asset for the U.S. semiconductor ecosystem, the NSTC is likely to have many missions and technical focus areas over the course of its existence. These missions and technical focus areas may require different sets of stakeholders and varying levels of engagement amongst them. The NSTC's bylaws should enable it, periodically, to review its governance and stakeholders to ensure that the NSTC continues to be well-equipped to succeed in its missions.

There is much more that the NSTC can learn from the organizations studied for this paper, but the learnings detailed above provide a solid foundation for effective governance of the NSTC. Without careful attention to governance, the best-laid plans in other areas (e.g., technical missions, budgeting, fund design, etc.) will be of little consequence because the NSTC will not be able to execute them effectively and strategically. However, thoughtful design of the NSTC's governance will prepare the organization to be a valuable national resource for years to come.

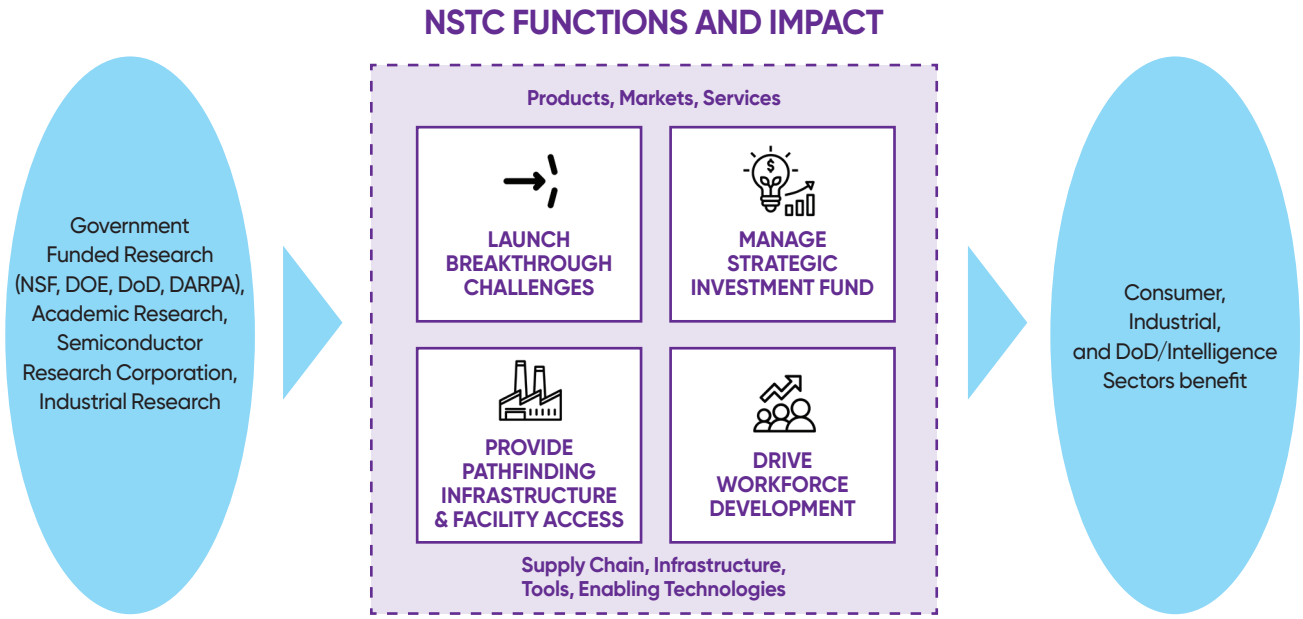

EXHIBIT 6: MUTUALLY REINFORCING CORE FUNCTIONS OF THE NSTC

Defining the Core Functions of the NSTC

In order to achieve maximum impact, all of the NSTC's core functions – launching Breakthrough Challenges, managing a strategic investment fund, providing pathfinding infrastructure and facility access, and driving workforce development – need to be mutually reinforcing. **Exhibit 6** illustrates our vision for how all of these functions can fit together effectively.

The following sub-sections provide more detailed recommendations for each of these functions.

Launching Breakthrough Challenges to Stimulate Full-Stack Innovation

To ensure that the NSTC focuses on revolutionary objectives and aligns innovation across the stack around a common set of problems, the NSTC should launch a series of Breakthrough Challenges. A Breakthrough Challenge should be an ambitious technical objective that:

- When achieved, will have various applications of substantial importance to the U.S. economy and national security and which has the potential to generate spillover innovations along the way,
- Is focused on what will be the industry state-of-the-art roughly seven to twelve years from now, and
- Addresses problems that no one company or organization can solve on its own – that is, efforts that require collaboration across organizations.[23]

Breakthrough Challenges should be defined and executed through a simple, competitive process. Leveraging a Technical Advisory Committee comprised of experts from industry, academia, and government, the NSTC should vet and select technical objectives worthy

of becoming Breakthrough Challenges and allocate appropriate overall levels of funding for each of them. For each Breakthrough Challenge, there should be an open competition whereby organizations of various types and sizes (e.g., industry leaders, small companies, universities, and teams thereof) can submit proposals to prototype and to scale technologies aligned with that Breakthrough Challenge. Each Breakthrough Challenge competition should result in multiple funding awards. This multiple-award approach is important, both to ensure that the NSTC maximizes its chances of generating breakthrough technologies – as not all projects will succeed – and to ensure that the NSTC promotes innovation at and across various levels of the stack. To promote a full-stack approach to addressing the Breakthrough Challenges, the NSTC can work with successful proposal teams to build connections between their work and that of other teams, as well as connect them with other potential partners who could complement their innovations. While the NSTC can provide substantial portions of funding required to de-risk proposed work, the proposing entities should be required to contribute some portion of the funding for the work themselves to ensure sufficient commitment to following through on the work. To remove potential chilling effects on innovation, the rights for IP generated through Breakthrough Challenges will be structured to be favorable for commercialization by the companies who participate in the Breakthrough Challenges.

Given the ambitious, large-scale, long-term, high-risk nature of Breakthrough Challenges, it is unlikely that industry proposals to the NSTC will be comprehensive. In instances where there are critical gaps between proposals and what is required to achieve Breakthrough Challenges, the NSTC should have the ability to execute some work itself, drawing upon its own resources. A Technical Advisory Committee in the NSTC could play a significant role in determining when the NSTC should or should not execute work itself to ensure both that Breakthrough Challenges have maximum chances of success and that the NSTC does not over-extend itself. To understand how the NSTC might invest strategically in filling gaps in Breakthrough Challenges itself, consider SEMATECH's involvement in developing extreme ultraviolet lithography (EUVL) in **Exhibit 7** on the next page.

Extreme ultraviolet lithography (EUVL) gained broad attention as a promising lithography technique in the 1980s. Early R&D programs and partnerships undertaken by industry and government advanced key enabling technologies and highlighted additional R&D gaps that needed to be filled in order to make EUVL a reality. Among these early efforts were investments in EUV reflectometry by NIST and DARPA, as well as investments in the development of source and microexposure tools by Sandia, Lawrence Livermore, and Lawrence Berkeley National Laboratories, Intel, AMD, and Motorola. Ultimately, SEMATECH took on the challenge of leveraging this fundamental R&D to create actual fabrication technology that could achieve nanometer scaling of transistor elements. SEMATECH had to make substantial investments for over a decade and a half before EUVL arrived in manufacturing in 2019. SEMATECH contracted with existing companies to leverage necessary infrastructure and expertise, and it built new infrastructure where there were gaps that industry considered to be too risky to fill on its own.

Below is a rough breakdown of the investments that SEMATECH had to make in infrastructure and access to existing facilities and tools:

- **EUV imaging access:** $300M-$500M; two generations of early model alpha and beta tools at IMEC and Albany, advanced light sources at Lawrence Berkeley National Laboratory and the Paul Scherrer Institute
- **EUV mask blank manufacturing:** $100M; developed by SEMATECH
- **EUV metrology:** $100M; Zeiss alpha model funded by SEMATECH
- **EUV resists:** $500M; developed through scanner access at Japanese companies, Dow/Dupont, Inpria, and Irresistible Materials
- **EUV imaging:** $100M; dedicated beam lines and end stations at Lawrence Berkeley National Laboratory

The key takeaway is that while SEMATECH made use of contracts to leverage existing infrastructure, it did not solely rely on the companies and research institutes that it contracted to achieve the objective of commercializing EUVL. Instead, it owned the responsibility and risk to execute on its mission and undertook the task of building the infrastructure and proving out the concepts (e.g., EUV mask blank manufacturing) that no other organization was willing to undertake.

EXHIBIT 7: SEMATECH'S PROJECT EXECUTION AND INFRASTRUCTURE STRATEGY FOR EUVL

The idea of the U.S. government's launching Breakthrough Challenges in partnership with industry to catalyze domestic innovation in sectors critical to U.S. economic and national interests has some notable precedents. The National Aeronautics and Space Administration (NASA) used a similar model for its Commercial Orbital Transportation Services (COTS) program to spur the development of a domestic capability to launch cargo and crews to the International Space Station (ISS), thereby reducing the U.S.'s dependency on Russia for launch capabilities.[24] See **Exhibit 8** for more details on best practices from the COTS program. Similarly, in 2017, the Obama Administration's President's Council of Advisors on Science and Technology (PCAST) recommended taking a "moonshot" approach to public-private collaboration on semiconductor innovation.[25]

Industry has already identified some of the key imperatives for next-generation semiconductor innovation that can inform these Breakthrough Challenges through the Semiconductor Research Corporation's *Decadal Plan for Semiconductors*. **Exhibit 9**, on the next page, shows a table that summarizes SRC's five "seismic shifts" in the semiconductor industry that require breakthrough innovation, along with examples of technologies that illustrate types of work that could potentially fall under an NSTC Breakthrough Challenge.

Breakthrough Challenges can provide the focus, coordination, and de-risking necessary to turn promising ideas in the lab into full-stack, fab-ready innovations that drive American growth.

NASA's Commercial Orbital Transportation Services (COTS) program – which ran from 2006 to 2013 – successfully leveraged $500M in government funding to catalyze the creation of a domestic capability to transport cargo to low-earth orbit. By 2013, both SpaceX and Orbital Sciences Corporation had executed successful resupply missions to the International Space Station (ISS). Below are some of the best practices that enabled the COTS program's success:

- **Specify Objectives, Not Approach:** NASA provided companies with a clear set of target capabilities and objectives but did not place numerous requirements on how companies approached them. This flexibility allowed companies to be creative and to develop solutions that made technical and commercial sense.
- **Co-Invest:** NASA did not provide all of the funding for awardees' projects. Instead, they required that awardees contribute a portion of the overall funding required for their projects. This requirement incentivized companies to develop solutions that would be commercially viable and increased their motivation to succeed.
- **Invest in Multiple Approaches:** COTS made awards to multiple companies that took diverse approaches to achieving the program's objectives. As a result, NASA's objectives did not depend on the success or failure of any one idea or team. Competition of ideas and approaches also motivated companies to develop the best solutions possible.
- **Let Industry Retain IP:** NASA agreed to let participating companies retain the IP they created to avoid potential chilling effects on innovation and to ensure that companies could serve commercial markets effectively.

EXHIBIT 8: NASA COTS PROGRAM[26, 27]

Seismic Shift	Description	Example Technologies
Smart Sensing	**"Fundamental breakthroughs in analog hardware are required to generate smarter world-machine interfaces that can sense, perceive, and reason"** **Goal:** "[T]o pursue analog-to-information compression/reduction with a practical compression/reduction ratio of 10^5:1 for practical use of information more analogous to the human brain"	· Domain-specific architectures targeting image, video, audio, radio frequency (RF) spectrum sensing applications · New sensor structures for sensitive applications in chemicals, gas, and biology — in several cases, the research has demonstrated viability, but scaling remains an issue · Sensor fusion to combine signals across sensor arrays or multiple types of sensors · Packaging for advanced sensors and heterogenous integration to optimize size, performance, power, and cost · Low-power edge AI to support data filtering and aggregation
Memory & Storage	**"The growth of memory demands will outstrip global silicon supply, presenting opportunities for radically new memory and storage solutions"** **Goal:** "[T]o develop emerging memories/ memory fabrics with > 10-100x density and energy efficiency improvement for each level of the memory hierarchy. Discover new storage systems and storage technologies with > 100x storage density capacity"	· Memory-centric compute encompassing near-memory compute, in-memory compute, and AI and neural-network compute that take advantage of analog and analog-like devices · Heterogeneous integration of new architected technologies at functional and physical levels to enable memory-centric compute · Novel device, design, architecture, software, etc., as well as technology solutions for architected systems in multi-tier and multi-chip stacking with innovative methods for integration materials
Communications	**"Always available communication requires new research directions that address the imbalance of communication capacity vs. data-generation rates"** **Goal:** "[E]nabling data movement of 100-1000 zettabyte/year at the peak rate of 1Tbps@ <0.1Nj/bit. Develop intelligent and agile networks that effectively utilize bandwidth to maximize network capacity"	· Digital and analog chips for ultra-high bandwidth radio and optical transmission for secure short- and long-distance communications · Semiconductor technologies for power-efficient optical, mmWave, and distributed agile secure network architectures · Combining smart sensors, edge cloud/compute, and on-device AI for end-to-end efficient communications network performance
Security	**"Breakthroughs in hardware research are needed to address emerging security challenges in highly interconnected systems and AI"** **Goal:** "[P]rivacy and security hardware advances that keep pace with new technology threats and use cases (e.g., trustworthy AI systems, secure hardware platforms, and emerging postquantum and distributed cryptographic algorithms)"	· Secure silicon supply chains, including quantifiable assurance, secure design flows, and verifiably secure layout-to-mask design flow[28] · Attestation systems for firmware and software, as well as ledger systems to track components throughout design and supply chain · Physical anti-tampering technology and technology to prevent access to secure information as products are disposed of or recycled
Energy Efficiency	**"Ever-rising energy demand for computing vs. global energy production is creating new risk, and new computing paradigms offer opportunities to dramatically improve energy efficiency"** **Goal:** "[T]o discover computing paradigms/ architectures with a radically new computing trajectory demonstrating >1,000,000x improvement in energy efficiency"	· Computing architectures and breakthrough technology in devices and operational software for cloud computing and AI to reduce energy consumption dramatically · Heterogenous integration of compute, storage, and data input/output (I/O) for optimization of energy and thermal benchmarks · Next generation of materials and technologies like two-dimensional materials, cold CMOS, and cryo CMOS-based lower-power integrated circuits

EXHIBIT 9: SEISMIC SHIFTS FROM SRC'S ***DECADAL PLAN FOR SEMICONDUCTORS***[29] AND EXAMPLE TECHNOLOGIES

Managing a Strategic Investment Fund

The 2021 NDAA – which calls for the creation of a semiconductor investment fund – provides a unique opportunity to fulfill early-stage companies' critical, unmet need for capital. Leveraging public funding, alongside private capital (as shown in **Exhibit 10**), the NSTC investment fund could take risks that the marketplace is unwilling to take on its own. The NSTC can increase the capital flow to semiconductor startups not only by making investments itself, but also by de-risking the journeys of early-stage companies through the valley of death by providing engineering services, wafer starts, facility access, and connections to potential partners and customers. By lowering startups' risk profile, the NSTC will make these companies more attractive to a wide range of investors.

While NSTC management will need to undertake deeper analysis to define the size and terms of its investment deals to best fill unmet market needs, there is still much that can be said now about how the fund ought to operate.

First, the NSTC investment fund should not be limited to specific types of semiconductors (e.g., only advanced logic) but should consider investments in organizations pursuing any next-generation semiconductor technology consistent with the level of ambition and projected impact of the NSTC's Breakthrough Challenges.[30] This is not to say that investments should only be tied to the particular Breakthrough Challenges the NSTC pursues, but, rather, that they should share the same revolutionary mindset.

Second, the NSTC investment fund should work closely with the Breakthrough Challenges arm of the NSTC, universities, DARPA, National Laboratories, SRC, etc. to identify startups emerging out of basic research that the NSTC should consider shepherding through the valley of death. Rather than duplicating the missions of other organizations, the NSTC should enhance them by funding and guiding the transition of their innovations out of the lab.

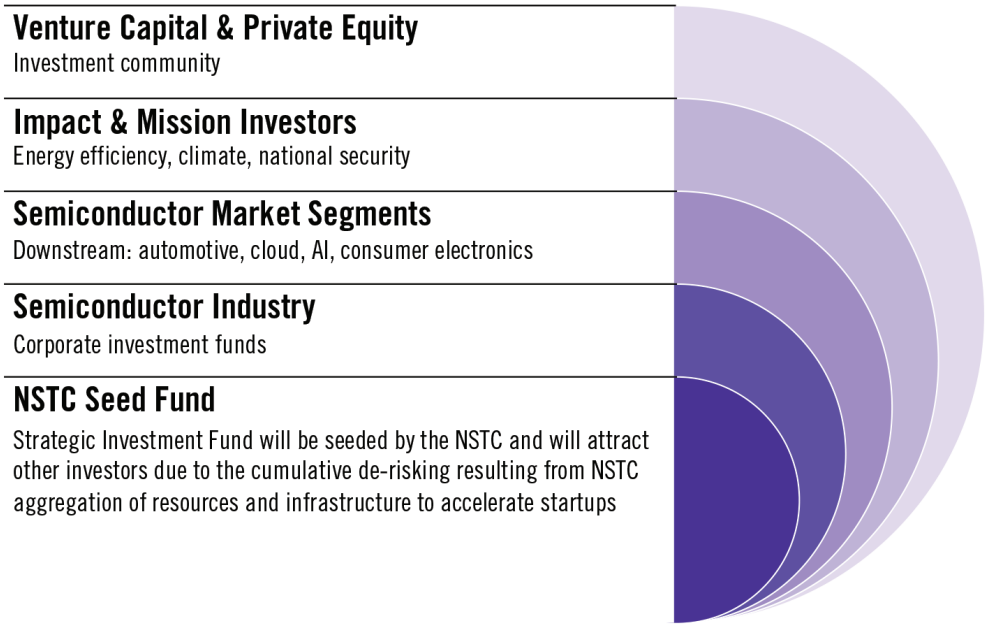

EXHIBIT 10: STRATEGIC INVESTMENT FUND

Finally, the NSTC investment fund should operate like an incubator, providing hands-on and in-kind support to startups, where necessary, to help them succeed. The NSTC should actively connect the companies it funds with the larger, established entities that participate in other aspects of the NSTC's mission, such as the Breakthrough Challenges. This can help startups build relationships with potential customers and enable larger companies to see what new technologies they need to prepare to integrate into their own roadmaps. When needed, the NSTC should make in-kind investments in startups in the form of access to key facilities, wafer runs, etc. The following section provides greater detail about how the NSTC should coordinate, create, and manage infrastructure assets to enable this approach, in addition to supporting the Breakthrough Challenges.

Providing Pathfinding Infrastructure and Facility Access

To begin making an impact as quickly as possible and to use its resources most effectively, the NSTC should leverage relevant existing facilities from across the nation, constructing or acquiring new infrastructure, as needed, to fill critical gaps. New fab facilities can cost several billion dollars and take years to build, and the U.S. cannot afford to wait that long for the NSTC to begin creating impact.

Fortunately, many of the facilities and tools that both large companies and startups need to refine their innovations for production-readiness already exist in the U.S. – the challenge is accessing those facilities. The NSTC can play a critical role in supporting the nation's innovation capacity by providing fair and easy access to a range of facilities and infrastructure, both in the context of NSTC-sponsored Breakthrough Challenges and startup investments, as well as private projects funded by organizations that would like to do their prototyping and scaling in the U.S. Where possible, large corporations with suitable facilities should also be able to perform Breakthrough Challenge work in their own facilities with their own technical staff. Smaller organizations and startups are more likely to need assistance accessing facilities appropriate for their work. Startups interviewed for this paper reported that relying on contract user facilities can be risky for them because they can lose their reserved fab access to larger companies that are willing to pay more and run higher volumes of wafers. They also often struggle to gain access to existing commercial fab facilities due to the lack of incentives for managing organizations to make these facilities accessible to them. There are three ways the NSTC should help organizations – both large and small – gain access to the facilities they need to conduct their Breakthrough Challenge work or to grow their businesses:

Connecting organizations to manufacturing facilities and negotiating access to those facilities

The NSTC should leverage its connections and resources to coordinate access to existing and future U.S. facilities. Such coordinated access could include the purchasing of wafer starts for multi-project wafer runs at fabs. The facilities to be constructed with resources from Section 9902 of the 2021 NDAA should be included in the network of accessible infrastructure for the NSTC. For startups, the NSTC's help in negotiating access to facilities could be an in-kind investment that results in NSTC equity stake in the companies. For Breakthrough Challenge participants, the NSTC's coordination of facility access could be considered part of the NSTC's funding award.

Creating annexes at existing fabrication facilities

One lower-cost alternative to building new facilities is to fund the creation of annexes at existing or future facilities (such as those built with Section 9902 resources) with the condition that they be available for NSTC use. An annex is an addition to an existing manufacturing facility created to increase the capability of the facility. NSTC annexes would be focused specifically on building the pathfinding infrastructure necessary to transition concepts to high-volume manufacturing. There are multiple advantages to creating annexes:

- First, annexes allow innovators working on scaling their technologies to work in the sort of environments and with the processes and tools that will ultimately be used to manufacture their end-products. This makes it easier and more efficient to transition technologies into production when they are ready for market.
- Second, annexes are efficient in terms of cost. Annexes leverage the existing process equipment, workforce, campus utility infrastructure, and surrounding semiconductor ecosystem (e.g., gas and chemical suppliers, equipment suppliers, etc.), while expanding the attributes of the facility that are necessary for prototyping and scaling next-generation devices.
- Third, leveraging multiple annexes would allow the NSTC to work across a diverse set of semiconductor technologies. For example, an annex associated with a 300 mm silicon wafer fab could be used for research into next-generation memory and logic devices, and another annex associated with a four-inch compound semiconductor fab could be used for research into photonics and RF devices. Annexes could also be designed and constructed to enable them to be upgraded, adapted, and expanded over time as technologies and technical missions evolve.

Establishing NSTC-owned infrastructure by purchasing and retooling existing facilities opportunistically or by building new facilities

Another less expensive alternative to building new facilities from the ground up is acquiring existing fab or packaging facilities that companies are looking to sell and retooling them for other purposes, as needed. Arizona State University took this approach when it acquired a Motorola fab facility to establish its MacroTechnology Works center.

Ultimately, if it becomes necessary to build a new facility to achieve important technical missions, the NSTC should have the option to do so. However, given the large expense and time commitment involved in building an entirely new facility, the NSTC should look first to other creative solutions, like those described above.

Driving Workforce Development

To support domestic invention, scaling, and production of semiconductor innovations, the U.S. needs to make substantial investments in developing and sustaining a robust semiconductor workforce. A 2017 survey conducted by Deloitte and SEMI found that 82% of semiconductor industry executives reported a shortage of qualified job candidates.[31] The challenge of finding qualified workers exists at all skill and education levels, from technicians to doctoral-level engineers. While there are already some programs designed to address the workforce gap – notably SRC's graduate fellowships, student research opportunities, and assistance for students seeking internships and job opportunities – there is much more

to be done to ensure that the U.S. has the workforce it needs to lead the next generation of semiconductors.[32] **Exhibit 11** illustrates the importance of semiconductor education and jobs to the nation as a whole by mapping the current semiconductor employment per state and the locations of current SRC participating universities.

There are four important roles that a nationwide NSTC workforce development program could – and should – have to help build a robust U.S. semiconductor workforce for the coming decades:

Develop enhanced university curricula that prepares students for semiconductor careers

Most engineering positions in semiconductor companies – even entry-level positions – require specialized skills and knowledge that are not necessarily covered in standard university coursework in electrical, materials, or computer engineering or physics. The NSTC should work with industry and academia to develop revitalized curricula and associated experimental resources in integrated circuit and systems design, semiconductor materials, devices, and microfabrication technology that will prepare students to join the semiconductor workforce and to contribute to the next generation of semiconductor technologies.

Provide hands-on training

The NSTC should sponsor internships and fellowships (undergraduate, graduate, and post-doctoral) to provide university students with hands-on experience in the design of semiconductor devices and integrated circuits, in microfabrication, in wafer processing tools, and in packaging. These internships and fellowships could involve working in the NSTC directly or

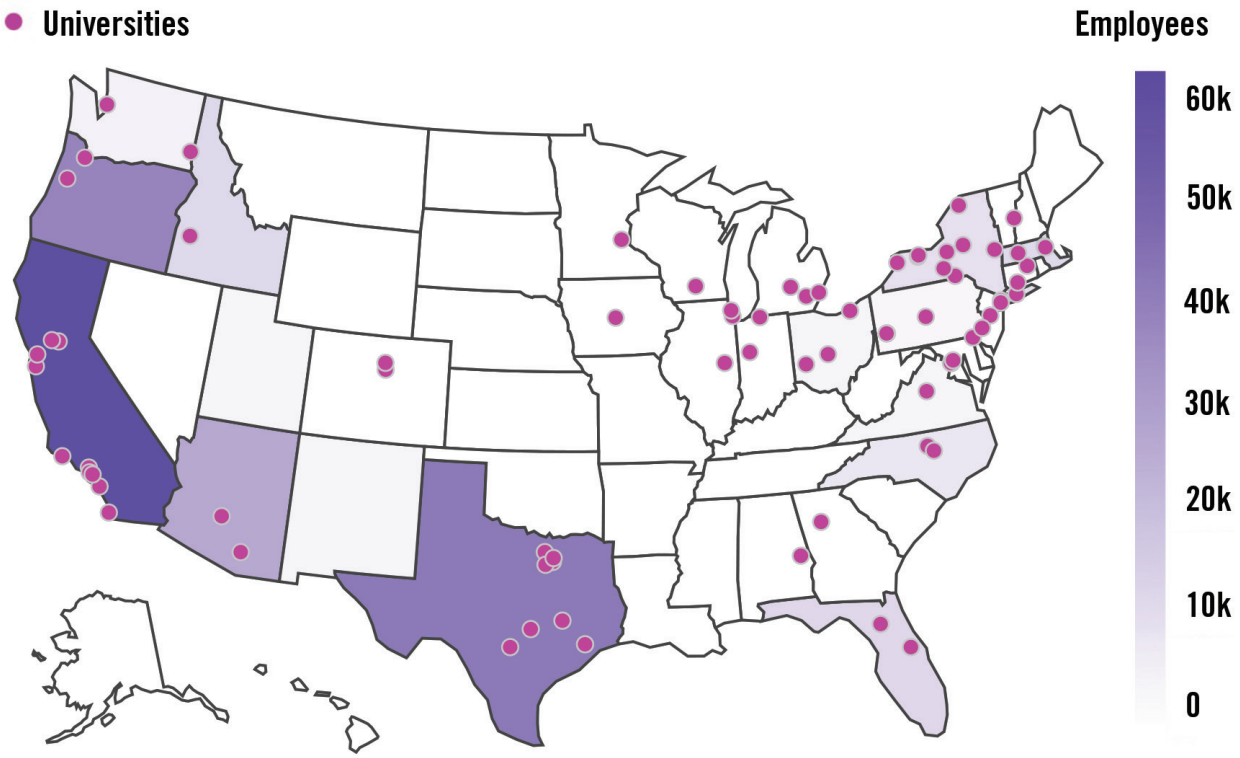

EXHIBIT 11: U.S. SEMICONDUCTOR EMPLOYEES PER STATE AND U.S. UNIVERSITIES WITH SEMICONDUCTOR PROGRAMS [33, 34]

at a company participating in a Breakthrough Challenge. Ideally, all Breakthrough Challenge proposals should include plans for including students in the execution of the work. One specific idea to consider is whether undergraduate and graduate internships and scholarship funding could be integrated into a semiconductor industry analogue to the Reserve Officers' Training Corps (ROTC) and the Department of Defense's (DoD's) SMART Scholarship, whereby students receive educational grants and experiences during undergraduate studies in exchange for a work commitment after graduation.[35, 36]

Enhance vocational training

The NSTC should also work with industry, community colleges, and vocational schools to develop and to enhance curricula for training programs for technicians critical to semiconductor manufacturing. To the extent that the NSTC owns and operates its own facilities, it should provide apprenticeship and other training programs for vocational students directly.

Inspire K-12 students to study to become semiconductor professionals

In order to have a robust semiconductor workforce in the coming decades, it is critical to build a pipeline of students interested in Science, Technology, Engineering, and Mathematics (STEM) – and in semiconductors in particular – at the primary and secondary level. High-profile scientific and technical challenges like the Space Race and the Human Genome Project inspired generations of young students to learn about space and biology and, ultimately to pursue careers in aerospace and biotechnology. With its mission of catalyzing and driving Breakthrough Challenges, the NSTC will be in a unique position to define what the Space Race or Human Genome equivalents are for next-generation semiconductor innovation and to develop campaigns to inspire young students to contribute to those breakthroughs. The NSTC's campaigns should involve K-12 lesson plans about Breakthrough Challenges and the importance of semiconductors in technology and society, grade level-appropriate hands-on activities, teacher programs, and school speakers. It is also important for the NSTC to publicize its internship, fellowship, scholarship, and career opportunities to high school students so that they know there are clear and exciting steps they can take toward a career in the semiconductor industry.

The recommendations above are far from the only steps that need to be taken to ensure that the U.S. has a robust semiconductor workforce for decades to come. Of at least equal importance are immigration policy reforms that allow foreign students studying at U.S. universities to pursue careers in the semiconductor industry here, rather than abroad.[37] Depending upon the specific field and degree level, non-U.S. nationals make up between 50 and 75% of students in relevant graduate engineering programs at U.S. universities.[38] Thus, retaining these students as part of the U.S. workforce is vitally important to enhancing U.S. competitiveness. While the NSTC cannot directly address this issue through policy, it could provide an attractive U.S.-based employment opportunity for competitive graduates from U.S. degree programs, potentially incentivizing those students to stay in the U.S. The NSTC can play several valuable roles in growing the domestic workforce the U.S. needs to drive long-term semiconductor leadership, but it must do so as part of a larger supporting ecosystem.

Defining Success for the NSTC

The 2021 NDAA states that, the U.S. semiconductor strategy must "(I) accelerate the domestic development and production of microelectronics and strengthen the domestic microelectronics workforce; and (II) ensure that the United States is a global leader in the field of microelectronics research and development."[39] However, the NDAA does not specify metrics for evaluating the NSTC's progress against these objectives.

As clear objectives and metrics are critical to the success of any substantial undertaking, we propose the following set of metrics (**Exhibit 12**) for the evaluation of the NSTC's work. To develop these metrics, we considered the objectives and outcomes of other successful government programs centered around complex technical moonshots in industries critical to U.S. competitiveness (e.g., Energy Efficient Engine program, NASA COTS, and the Human Genome Project).

During the proposal process and establishment of the NSTC, these metrics should become more specific and measurable. This is critical to ensure that the NSTC can be held accountable to advancing U.S. leadership, resiliency, and security for decades to come.

EXHIBIT 12: METRICS FOR SUCCESS

Positioning the NSTC for Sustained Impact

Investing with Realistic Expectations

To sustain the impact of initial investments, the NSTC must rally both industry and government to provide ongoing support, funding, and resources. None of the past or existing organizations that we have studied (see **Exhibit 5**) has managed to become completely self-sustaining. Imec has come the closest to being self-sustaining, but it has been in existence for decades and was still primarily dependent on government funding five years into its existence.[40] It is highly unlikely that the NSTC, by contrast, could become self-sustaining within a few years. Moreover, given that cutting-edge tools can cost tens of millions of dollars – even hundreds of millions in the case of lithography tools – it would be difficult for the NSTC ever to retain enough earnings to keep pace with evolving technology without continued investment.

Coordinating with Other U.S. Investments

To be successful, the NSTC must work in concert with other NDAA investments in the semiconductor industry, as well as with the existing ecosystem of semiconductor R&D in the U.S. NSTC coordination with other 2021 NDAA investments should include:

- Section 9902 calls for Manufacturing Incentive Grants to be awarded by the Dept. of Commerce "to incentivize investment in facilities and equipment in the United States for semiconductor fabrication, assembly, testing, advanced packaging, or research and development." These new facilities should be required to demonstrate how they will work with the NSTC to transition new technologies to domestic manufacturing. For example, applicants for the incentive grants could be required to develop plans for (i) constructing NSTC annexes adjacent to new manufacturing facilities, (ii) coordinating access for NSTC-funded startups or Breakthrough Challenge participants, and/or (iii) ensuring capacity is available for the NSTC to purchase wafer starts and other capabilities.
- Section 9903 calls for a National Network for Microelectronics Research & Development (NNMRD) to be established by the DoD to enable "laboratory to fabrication transition of microelectronics innovations in the United States." The establishment of the NNMRD will likely involve augmenting and building capabilities at the leading research universities and laboratories in the U.S. As such, the NNMRD is an essential partner organization for the NSTC and will enable the U.S. research community to increase the volume of good ideas in the research pipeline that can (i) be funded under NSTC Breakthrough Challenges, (ii) be spun out into startups with NSTC investment and enablement, and (iii) be leveraged for NSTC workforce development programs.
- Section 9906 calls for the Department of Commerce to establish an Advanced Packaging Manufacturing Program (APMP). We recommend including the APMP as part of the NSTC because advanced packaging technologies are essential and increasingly inseparable from advances in semiconductor devices. Such consolidation would also reduce the redundancy, excess overhead costs, and duplicate governance structure that establishing a packaging program entirely separate from the NSTC would entail.

The NSTC should also coordinate with existing U.S. programs that support the national semiconductor ecosystem to ensure that they are mutually reinforcing. Programs like DARPA's and SRC's Joint University Microelectronics Program (JUMP) and Electronics Resurgence Initiative (ERI & ERI 2.0), DOE's microelectronics initiatives and facilities, the National Institute of Standards and Technology's (NIST's) microelectronics and metrology efforts, and NSF's National Nanotechnology Coordinated Infrastructure (NNCI) drive advances in basic and applied sciences that will need to be prototyped and scaled through the NSTC. Recent DoD projects – including the State-of-the-Art Heterogeneous Integrated Prototype (SHIP) program, the Rapid Assured Microelectronics Prototypes (RAMP) Project, and RAMP-Commercial (RAMP-C) – focus on developing industry capabilities that can have both government and commercial applications. The NSTC can help accelerate the commercialization of these capabilities.

Strengthening the U.S. National Security Posture

To succeed in enhancing U.S. economic resiliency and national security, the NSTC must respond to the needs of the DoD and the Intelligence Community, whose systems and mission capabilities depend on a range of microelectronics. DoD and Intelligence Community systems must operate in harsh and extreme environments well beyond commercial specifications. In addition to logic and memory, they have specialized needs in areas that include analog, RF, and mixed-signal waveform generation, detection, and processing (e.g., GaAs, GaN, SiGe) for radar, electronic warfare, and communications in highly contested environments; radiation hardened electronics; microelectronics assurance; access to leading-edge microelectronics; and security. The NSTC's portfolio of Breakthrough Challenges, startups, and pathfinding infrastructure will support these DoD and Intelligence Community needs.

Creating a Holistic Strategy to Sustain U.S. Leadership

Securing U.S. leadership in the next generation of semiconductors is imperative as technology and economic power emerge as modern battlegrounds. While the NSTC holds great promise, it cannot secure U.S. leadership in the next generation of semiconductors on its own. It is critical that the U.S. also consider and address other policy factors that historically have contributed to the offshoring of semiconductor production and that affect the attractiveness of the U.S. as a home base for new companies. Factors like tax policy and its impact on capital-intensive and asset-heavy businesses, export controls, environmental permitting regulations, Committee on Foreign Investment in the United States (CFIUS) reviews, and immigration pathways for skilled workers all merit careful analysis.[41] Without a supportive policy environment to complement the NSTC, promising technologies will still leave the U.S. to be developed and commercialized elsewhere – perhaps just after they have reached higher technical readiness levels than before the NSTC's creation.

The U.S. needs a holistic, whole-of-government approach to ensuring that the investments made through the 2021 NDAA can create maximum impact for U.S. industry. The establishment of an effective NSTC is the first of many steps the U.S. must take to ensure that American innovation leads to American growth for decades to come.

Conclusion and Call-to-Action

The 2021 NDAA's call to create a National Semiconductor Technology Center is a unique opportunity to strengthen the U.S.'s ability to translate American innovation into American growth. To deliver on this promise, the NSTC must be designed and established strategically, breaking with historical norms to capitalize on the realities of the modern global semiconductor supply chain. SEMATECH, the renowned U.S. industry consortium, was felled by many factors, including its inflexible and conflicted governance. Imec, the Belgian organization established in 1984, is the current global standard for collaborative industry R&D and a valuable partner to the whole industry. However, the presence of this leading R&D fabrication facility has not resulted in strong commercial semiconductor production in Europe. The NSTC must learn from these, and other, organizations and take action in radically new directions of technology and business practice that augment the innate strengths of the U.S. semiconductor ecosystem.

In this paper, MITRE Engenuity and The Semiconductor Alliance have presented the principles that should shape the establishment of the NSTC to catalyze future American leadership. The NSTC must embrace a bold technology agenda by investing in a portfolio of new ideas, including Breakthrough Challenges, and ensure that innovations have a pathway to domestic production through infrastructure access and a talented U.S. workforce. Leveraging our objectivity and independence, MITRE Engenuity and The Semiconductor Alliance are prepared to build an NSTC that reflects these recommendations and enhances the U.S.'s ability to translate American innovation into American growth.

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10. While the Fiscal Year 2021 National Defense Authorization Act (NDAA) was passed by Congress and became law, funding to implement the related semiconductor investments has not yet been appropriated by Congress as of the writing of this paper.
11. United States, Congress. Public Law 116-283, "William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021," §9906 (c)(1).
12. United States, Congress, Senate. United States Innovation and Competition Act of 2021 (USICA), S.1260 (117th Congress), as of June 8, 2021. Note that this $10.5 billion covers §9906 (c)-(f) of the FY 2021 NDAA, which encompass the NSTC, the National Advanced Packaging Manufacturing Program, National Institute of Standards and Technology (NIST) microelectronics R&D, and a new Manufacturing USA Institute. As the USICA bill has not been passed as of the writing of this paper, actual appropriations may differ from current expectations.
13. "Prototype" is defined as a functional demonstration of an original concept that spans the compute stack and is done in the context of a path to production and market drive.
14. "Scale" is defined to include the activities needed to generate statistically significant data for a prototype and to identify paths to manufacturability, areas for technology development, and risks to adoption for a prototype.
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